中華民國專利報 (19)(12)

(11)公告編號：347613

(44)中華民國87年(1998)12月11日

發明 全4頁

(51)Int.Cl.[6]：H03K7/08

第 90114545 號
初審
再審 (訴願)引証附件

(54)名稱：脈波信號產生器

(21)申請案號：86100562 (22)申請日期：中華民國86年(1997)01月20日

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[57]申請專利範圍：

1.一種脈波信號產生器，其包含：

一輸入端子以接收一預定時鐘頻率的參考時鐘信號；

一輸出端子以提供一有預定時鐘頻率框的輸出信號，每個框包含預定數目個隨機頻率之時間片段；

一鎖相迴路(PLL)，其有：

一相位偵測器，其有第一輸入連結到輸入端以接收一參考時鐘信號，第二輸入以接收回授信號，以及一輸出，相位偵測器係配置來將參考時鐘信號的相位與回授信號的做比較並產生一表示著參考時鐘信號與回授信號的相位差別的相位誤差信號；

一連結到相位偵測器之輸出的低通濾波器，其接收相位誤差信號並從之產生一誤差電壓，

一連結到低通濾波器輸出的電壓控制振盪器(VCO)，其接收一誤差電壓，並產生由誤差電壓調整的預定頻率之時鐘方波信號，其中時鐘方波信號的預定頻率高於解析頻率，以及

一連結到VCO的除頻器，其接收來自VCO的時鐘分波信號，並將頻率除以一預定值來提供回授信號；

一連結到PLL的脈波控制器，其有第一輸入以接收來自VCO的時鐘方波信號，第二輸入以接收資料信號以及一輸出提供有預定時鐘頻率框的信號，但其中每個框包含了頻率高於解析頻率的時間片段，而時間片段中的脈波係由資料信號決定；以及

一切換電路，其有連結到控制器的輸出之第一輸入，及有連接到輸出端子的輸出來切換來自控制器的信號到輸出端子，這樣在每個框的最少起始部份期間內輸出信號中就不會包含來自控制器的信號，如此每個框上的輸出信號平均頻率解析頻率，而在每個框中輸出信號之脈波高-低比率則由資料信號決定。

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Abstract

Pulsed Signal Generator

A pulse width modulated (PWM) voltage generator includes a phase locked loop (PLL) for generating a clock square-wave signal at a frequency which is twice that of a desired resolution frequency of the PWM output signal. A PWM controller (14) receives the clock square-wave signal and a data signal and provides a PWM output having a duty cycle determined by the data signal at the frequency of the clock square-wave signal. A switching circuit coupled to the PWM controller (14) receives a signal from a frequency divider (16), which forms part of the PLL, and switches an output of the generator to be floating for the first half of the PWM frame cycle so that the PWM output signal does not include the PWM output from the PWM controller when the clock square-wave signal has non-uniform frequency. But, because of the doubled frequency of the clock square-wave signal, the average frequency of the PWM output signal is still at the desired resolution frequency and the duty cycle of the PWM output signal is as determined by the data signal.

FIG. 1

Pulsed Signal Generator

Field of the Invention

This invention relates to a pulsed signal generator, and more particularly to such a generator for producing Pulse Width Modulated (PWM) or Pulse Density Modulated (PDM) signals formed in an open loop with a uniform clock system.

Background of the Invention

For a number of applications, such as control of a picture on a monitor screen, it is desirable to have accurately controlled d. c. voltage levels. Such voltages are often provided by a PWM voltage generator, whose output is provided to a low pass filter which averages the PWM output to provide the d.c voltage level. The output of the PWM voltage generator is a pulse waveform, having a controlled duty cycle, which determines the d.c. voltage level. The duty cycle of the pulse waveform is controlled by a PWM controller, which receives, as one input, a clock square-wave signal having a frequency which is determined according to the resolution required by the application, and, as a second input, a data signal, which provides to the PWM controller the duty cycle information from, for example, a microcontroller (MCU), indicating to the PWM controller, how wide the pulse of the PWM output should be.

The clock square-wave signal is conventionally generated by a phase locked loop (PLL) formed by a phase detector receiving a system clock signal input to the PLL, a low pass filter, a voltage-controlled oscillator (VCO) generating the clock square-wave signal output from the PLL, and a frequency divider in a feedback path between the output of the VCO and the phase detector. The frequency divider divides the VCO output frequency by the resolution frequency value required for the predetermined resolution. The phase detector, as is well known, compares the phase of the system clock signal input with the phase of the frequency divided clock square-wave signal output and provides a phase error signal to the low pass filter, which provides an error voltage to the VCO to adjust the frequency of the clock square-wave signal generated.

However, the feedback mechanism causes the phase error signal from the phase detector to induce a frequency jitter in the VCO output causing it to be either ahead of or behind the system clock signal at the beginning of each cycle. This frequency jitter in the VCO output causes the duty cycle of the PWM output from the PWM controller to be non-linear with respect to the data signal from the MCU, such that, at the beginning of the system clock cycle, the duty cycle of the PWM output is greater than the desired duty cycle according to the data signal. This causes the d.c. voltage level to be higher than required.

Brief Summary of the Invention

The present invention therefore seeks to provide a pulse width modulated (PWM) voltage generator which overcomes, or at least reduces, the above-mentioned problems of the prior art.

Accordingly, in one aspect, the invention provides a pulsed signal generator comprising:

an input terminal for receiving a reference clock signal at a predetermined clock frequency;

an output terminal for providing an output signal having frames at the predetermined clock frequency, each frame consisting of a predetermined number of timeslots at a resolution frequency;

a phase locked loop (PLL) having:

a phase detector having a first input coupled to the input terminal for receiving the reference clock signal, a second input for receiving a feedback signal and an output, the phase detector being arranged for comparing the phase of the reference clock signal with that of the feedback signal and for producing a phase error signal representative of the difference between the phase of the reference clock signal and the feedback signal,

a low pass filter coupled to the output of the phase detector for receiving the phase error signal and generating an error voltage therefrom,

a voltage-controlled oscillator (VCO) coupled to the low pass filter for receiving the error voltage and for generating a clock square-wave signal at a predetermined frequency adjusted by the error voltage, wherein the predetermined frequency of the clock square-wave signal is higher than the resolution frequency, and

a frequency divider coupled to the VCO for receiving the clock square-wave signal from the VCO and dividing the frequency thereof by a predetermined value to provide the feedback signal;

a pulse controller coupled to the PLL and having a first input for receiving the clock square-wave signal from the VCO, a second input for receiving a data signal and an output for providing a signal having frames at the predetermined clock frequency, but wherein each frame consists of timeslots at a frequency higher than the resolution frequency with pulses within the timeslots as determined by the data signal; and

a switching circuit having a first input coupled to the output of the controller and an output coupled to the output terminal for switching the signal from the controller to the output terminal such that the output signal does not include the signal from the controller during at least an initial portion of each frame such that the frequency of the output signal averaged over each frame is the resolution frequency and the pulse high-to-low ratio of the output signal within each frame is as determined by the data signal.

In a preferred embodiment, the switching circuit switches the output terminal to be left floating for the remainder of each frame except for the portion during which it is coupled to receive the signal from the controller.

Preferably, the predetermined frequency of the clock square-wave signal is an integral value multiple of the resolution frequency, wherein the integral value is at least two.

In one embodiment, the switching circuit comprises a second input for receiving an integral value multiple of the reference clock signal, wherein the integral value is at least one.

The predetermined frequency of the clock square-wave signal is preferably twice the resolution frequency and the second input of the switching circuit receives the reference clock signal. The switching circuit preferably switches the signal from the controller to the output terminal only during a second half of each frame.

Preferably, the controller is a Pulse Width Modulated (PWM) controller and the output signal is a PWM signal. Alternatively, the controller is a Pulse Density Modulated (PDM) controller and the output signal is a PDM signal.

According to a second aspect, the invention provides a pulse width modulated (PWM) voltage generator comprising:

an input terminal for receiving a reference clock signal;

an output terminal for providing a PWM output signal at a desired resolution frequency;

a phase locked loop (PLL) having:

a phase detector having a first input coupled to the input terminal for receiving the system clock signal, a second input for receiving a feedback signal and an output, the phase detector being arranged for comparing the phase of the system clock signal with that of a feedback signal and for producing a phase error signal representative of the difference between the phase of the system clock signal and the feedback signal,

a low pass filter coupled to the output of the phase detector for receiving the phase error signal and generating an error voltage therefrom,

a voltage-controlled oscillator (VCO) coupled to the low pass filter for receiving the error voltage and for generating a clock square-wave signal at a predetermined frequency adjusted by the error voltage, wherein the predetermined frequency of the clock square-wave signal is higher than a desired resolution frequency of the PWM output signal, and

a frequency divider coupled to the VCO for receiving the clock square-wave signal from the VCO and dividing the frequency thereof by a predetermined value to provide the feedback signal;

a pulse width modulation (PWM) controller coupled to the PLL and having a first input for receiving the clock square-wave signal from the VCO, a second input for receiving a data signal and an output for providing a PWM output having a duty cycle determined by the data signal and a frequency higher than the desired resolution frequency of the PWM output signal; and

a switching circuit having a first input coupled to the output of the PWM controller and an output coupled to the output terminal for switching the PWM output from the PWM controller to the output terminal such that the PWM output signal does not include the PWM output from the PWM controller during at least an initial portion of each cycle of the reference clock signal so that the average

frequency of the PWM output signal is at the desired resolution frequency and the duty cycle of the PWM output signal is as determined by the data signal.

In one preferred embodiment, the switching circuit switches the output terminal to be left floating for the remainder of each reference clock cycle except for the portion during which it is coupled to receive the PWM output from the PWM controller.

Brief Description of the Drawings

One embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a schematic block diagram of a pulse width modulated (PWM) voltage generator in accordance with one embodiment of the invention; and

FIG. 2 shows waveforms of signals at different points in the embodiment of FIG. 1.

Detailed Description of the Drawings

Thus, as mentioned above, it is desirable to have accurately controlled d. c. voltage levels for control of a picture on a monitor screen. Such voltages are provided by a PWM voltage generator, whose output is provided to a low pass filter which averages the PWM output to provide the d.c voltage level. The output of the PWM voltage generator is a pulse waveform, as shown by waveform 50 in FIG. 2, whose duty cycle is controlled by a PWM controller 14, as shown in FIG. 1, which receives, as one input, a clock square-wave signal on node 7 having a frequency which is determined according to the resolution required by the application, and, as a second input, a data signal on node 17, which provides to the PWM controller 14 the duty cycle information from, for example, a microcontroller (MCU) (not shown), indicating to the PWM controller 14, how wide the pulse of the PWM output should be.

The clock square-wave signal is conventionally generated by a phase locked loop (PLL). As shown in FIG. 1, the PLL is formed by a phase detector 2 receiving a system clock signal input on node1 as input to the PLL, a low pass filter (LPF) 4 formed by resistor 6 and capacitor 10 , a voltage-controlled oscillator (VCO) 12 generating the clock square-wave output on node 7, and a frequency divider 16 in

a feedback path between node 7, the output of the VCO 12, and node 13, the input to the phase detector 2. The frequency divider 16 divides the frequency of the clock square-wave output from the VCO 12 on node 7 by a value N required to produce a desired frequency on node 7. The frequency (f_7) of the signal on node 7 is $f_1.2^N$, where f_1 is the frequency of the signal on node 1. The phase detector 2, as is well known, compares the phase of the clock signal on node 1 with the phase of the square-wave signal on node 7 and provides a phase error signal on node 3, as shown by waveform 51 in FIG. 2, at the input to the low pass filter 4, which provides an error voltage to the VCO 12 to adjust the frequency of the clock square-wave signal generated on node 7.

However, this feedback mechanism causes the phase error signal from the phase detector 2 to induce a frequency jitter in the VCO output on node 7 causing it to either lead or lag the system clock signal on node 1 at the beginning of each clock cycle.

Normally the phase detector output is of push-pull type. However, to ensure that the signal on node 7 always lags that on node 1 a phase detector 2 with open drain output is used together with resistor 8 which injects current into node 5. This arrangement produces a voltage on node 5 as shown by waveform 52 in FIG. 2. This voltage on node 5 will produce a signal of non-uniform frequency on node 7, the output of VCO 12, as shown by waveform 53 in FIG. 2. This frequency non-uniformity in the VCO output causes the time slots in PWM controller 14 to be of non-uniform period as shown in waveform 54 in FIG. 2, where time slot 01 is referenced 62 and time slot 2^M, where M is the number of data bits for the PWM controller14, is referenced 63. This results in a duty cycle of the PWM output on node 9 from the PWM controller 14 to be non-linear with respect to the data signal from the MCU input on node 17 to the PWM controller 14, such that, at the beginning of the system clock cycle, the duty cycle of the PWM output on node 9 is greater than the desired duty cycle according to the data signal. This causes the d.c. voltage level to be higher than required, hence introducing non-linearity in the output.

As an example, waveform 55 in FIG. 2 shows the voltage on node 9 for a data value of $01 and waveform 56 shows that for data

value of $02. It can be seen that the width of the pulse on waveform 56 is not twice that of the pulse on waveform 55.

To overcome this problem, the frequency divider 16 divides the frequency on node 7 by 2N so that the VCO 12 produces an output on node 7, as shown by waveform 57, which has a frequency twice that of the frequency required by the PWM controller 14. The signal on node 11, as shown by waveform 59, is used to control output enable logic formed by gates 18, 20 and 22. The signals on nodes 19 and 21 switch off transistors 24 and 26 during the high part of the signal on node 11 so that node 15 is floating. During the second half of the cycle of the signal on node 11, the output of the PWM controller 14 is passed through to the node 15. It will be appreciated that waveforms 57 - 61 in FIG.2 are expanded to show one frame of PWM cycle.

Waveforms 60 and 61 show the signal on node 15 for PWM data of $01 and $02 respectively. Since node 15 is left floating during period 64, shown on waveform 60, the output d.c voltage on node 23 has a mark/space ratio as shown by arrows 65 and 66 in waveform 60. This mark/space ratio is the same as that of waveforms 55 and 56 would have been had waveform 53 had a uniform frequency throughout the PWM cycle. Since the period of non-uniformity has now been removed, this results in a linear voltage on node 23 which is the output of the low pass filter formed by resistor 28 and capacitor 30.

As mentioned above, although the particular embodiment described above uses a pulse width controller to provide a PWM output signal, the invention is also applicable to systems using Pulse Density Modulation (PDM), where the output signal has a number of timeslots in which the density of pulses having equal widths determines the final voltage. Furthermore, although the particular embodiment described above doubles the PLL output frequency and then masks out half of each cycle of the PWM controller output, it will be apparent that the PLL frequency could be quadrupled, or indeed multiplied by any other integer, provided the PWM controller output that is passed to the output of the generator is a fraction of each cycle of the PWM controller output taken by dividing the cycle by the integer and using a fraction of the cycle

that does not fall within the non-uniform frequency region at the beginning of each PLL cycle.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various other modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

第 86100562 號專利申請案
英文申請專利範圍修正本 (87 年 8 月)
ROC (Taiwan) Patent Application No. 86100562
Amended Claims (August 1998)

1. A pulsed signal generator comprising:

a input terminal for receiving a reference clock signal at a predetermined clock frequency;

an output terminal for providing an output signal having frames at the predetermined clock frequency, each frame consisting of a predetermined number of timeslots at a resolution frequency;

a phase locked loop (PLL) having:

a phase detector having a first input coupled to the input terminal for receiving the reference clock signal, a second input for receiving a feedback signal and an output, the phase detector being arranged for comparing the phase of the reference clock signal with that of the feedback signal and for producing a phase error signal representative of the difference between the phase of the reference clock signal and the feedback signal,

a low pass filter coupled to the output of the phase detector for receiving the phase error signal and generating an error voltage therefrom,

a voltage-controlled oscillator (VCO) coupled to the low pass filter for receiving the error voltage and for generating a clock square-wave signal at a predetermined frequency adjusted by the error voltage, wherein the predetermined frequency of the clock square-wave signal is higher than the resolution frequency, and

a frequency divider coupled to the VCO for receiving the clock square-wave signal from the VCO and dividing the frequency thereof by a predetermined value to provide the feedback signal;

a pulse controller coupled to the PLL and having a first input for receiving the clock square-wave signal from the VCO, a second input for receiving a data signal and an output for providing a signal having frames at the predetermined clock frequency, but wherein each frame consists of timeslots at a frequency higher than the resolution frequency with pulses within the timeslots as determined by the data signal; and

a switching circuit having a first input coupled to the output of the controller and an output coupled to the output terminal for switching the signal from the controller to the output terminal such

that the output signal does not include the signal from the controller during at least an initial portion of each frame such that the frequency of the output signal averaged over each frame is the resolution frequency and the pulse high-to-low ratio of the output signal within each frame is as determined by the data signal.

2. A pulse signal generator according to claim 1, wherein the switching circuit switches the output terminal to be left floating for the remainder of each frame except for the portion during which it is coupled to receive the signal from the controller.

3. A pulse signal generator according to either claim 1 or claim 2, wherein the predetermined frequency of the clock square-wave signal is an integral value multiple of the resolution frequency, wherein the integral value is at least two.

4. A pulse signal generator according to claim 3, wherein the switching circuit comprises a second input for receiving an integral value multiple of the reference clock signal, wherein the integral value is at least one.

5. A pulse signal generator according to claim 4, wherein the predetermined frequency of the clock square-wave signal is twice the resolution frequency and the second input of the switching circuit receives the reference clock signal.

6. A pulse signal generator according to claim 5, wherein the switching circuit switches the signal from the controller to the output terminal only during a second half of each frame.

7. A pulse signal generator according to either claim 1 or claim 2, wherein the controller is a Pulse Width Modulated (PWM) controller and the output signal is a PWM signal.

8. A pulse signal generator according to either claim 1 or claim 2, wherein the controller is a Pulse Density Modulated (PDM) controller and the output signal is a PDM signal.

9. A pulse width modulated (PWM) voltage generator comprising:

a input terminal for receiving a reference clock signal;

an output terminal for providing a PWM output signal at a desired resolution frequency;

a phase locked loop (PLL) having:

a phase detector having a first input coupled to the input terminal for receiving the system clock signal, a second input for receiving a feedback signal and an output, the phase detector being arranged for comparing the phase of the system clock signal with that of a feedback signal and for producing a phase error signal representative of the difference between the phase of the system clock signal and the feedback signal,

a low pass filter coupled to the output of the phase detector for receiving the phase error signal and generating an error voltage therefrom,

a voltage-controlled oscillator (VCO) coupled to the low pass filter for receiving the error voltage and for generating a clock square-wave signal at a predetermined frequency adjusted by the error voltage, wherein the predetermined frequency of the clock square-wave signal is higher than a desired resolution frequency of the PWM output signal, and

a frequency divider coupled to the VCO for receiving the clock square-wave signal from the VCO and dividing the frequency thereof by a predetermined value to provide the feedback signal;

a pulse width modulation (PWM) controller coupled to the PLL and having a first input for receiving the clock square-wave signal from the VCO, a second input for receiving a data signal and an output for providing a PWM output having a duty cycle determined by the data signal and a frequency higher than the desired resolution frequency of the PWM output signal; and

a switching circuit having a first input coupled to the output of the PWM controller and an output coupled to the output terminal for switching the PWM output from the PWM controller to the output terminal such that the PWM output signal does not include the PWM output from the PWM controller during at least an initial portion of each cycle of the reference clock signal so that the average

frequency of the PWM output signal is at the desired resolution frequency and the duty cycle of the PWM output signal is as determined by the data signal.

10. A PWM voltage generator according to claim 9, wherein the switching circuit switches the output terminal to be left floating for the remainder of each reference clock cycle except for the portion during which it is coupled to receive the PWM output from the PWM controller.

11. A PWM voltage generator according to either claim 9 or claim 10, wherein the predetermined frequency of the clock square-wave signal is an integral value multiple of the desired resolution frequency of the PWM output signal, wherein the integral value is at least two.

12. A PWM voltage generator according to claim 11, wherein the switching circuit comprises a second input for receiving an integral value multiple of the reference clock signal, wherein the integral value is at least one.

13. A PWM voltage generator according to claim 12, wherein the predetermined frequency of the clock square-wave signal is twice the desired resolution frequency of the PWM output signal and the second input of the switching circuit receives the reference clock signal.

14. A PWM voltage generator according to claim 13, wherein the switching circuit switches the PWM output to the output terminal only during a second half of each reference clock cycle.

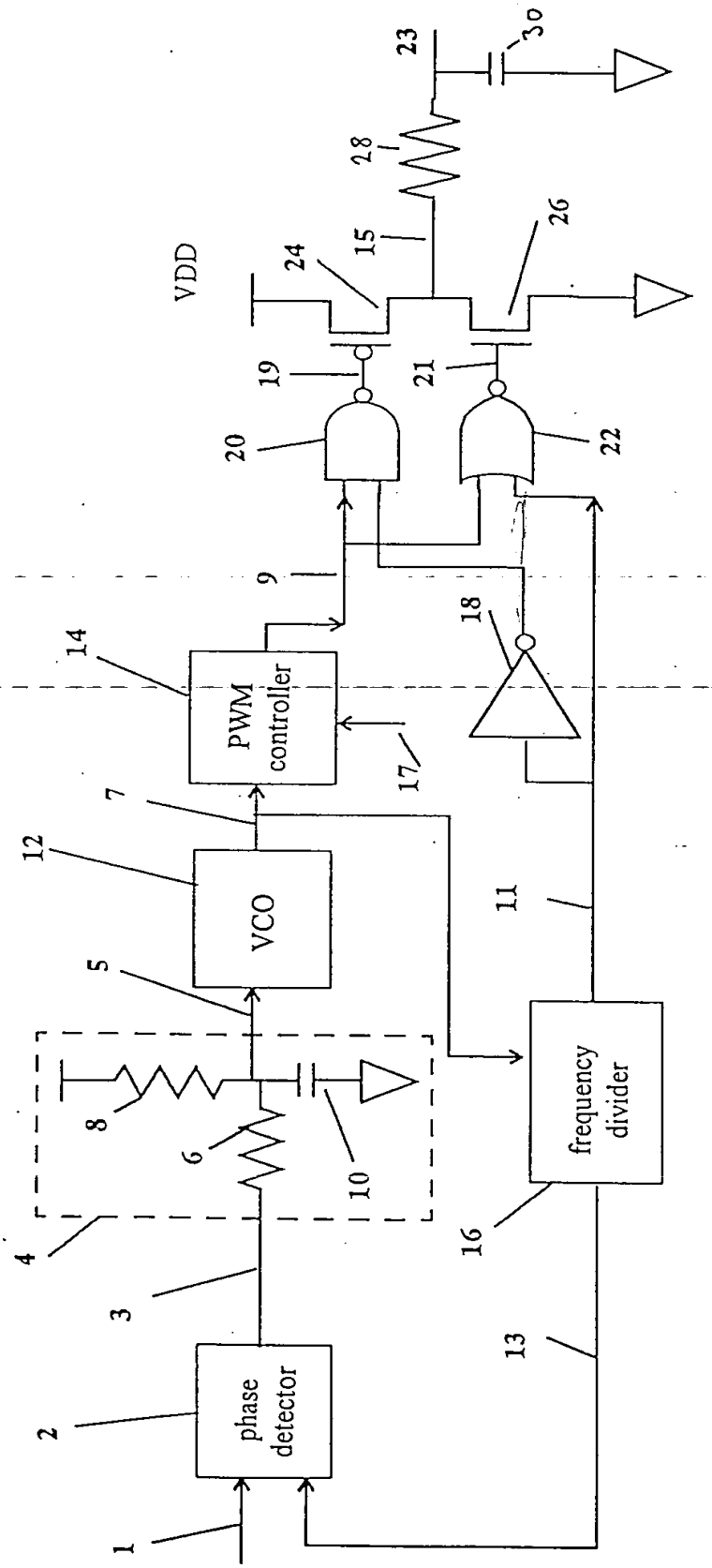
VDD
PWM controller
VCO
frequency divider
phase detector
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FIG. 1

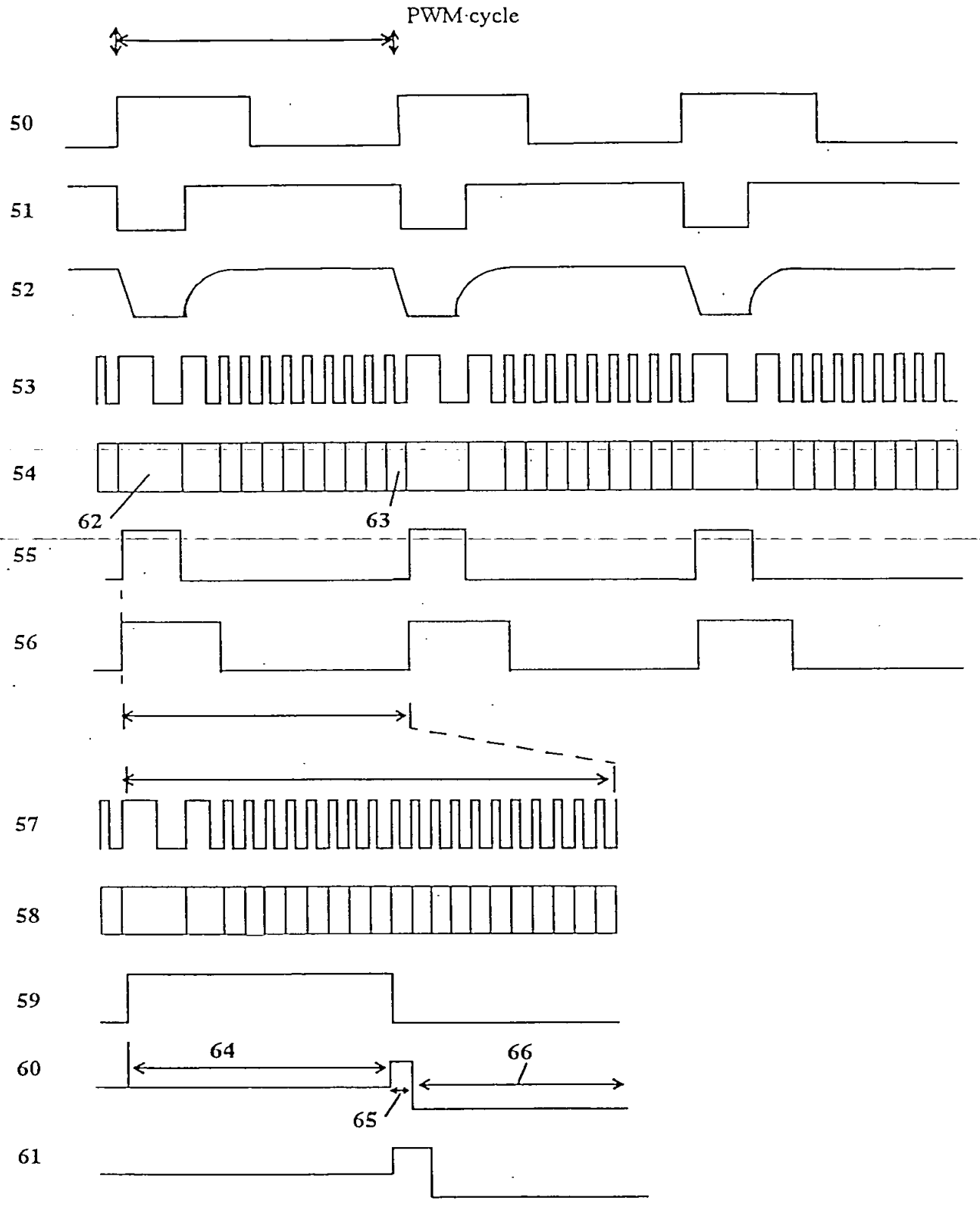

FIG. 2